REMARKS

This is in response to the Office Action dated September 3, 2004. In that Office Action, Examiner rejected claims 1-18 (all the claims) under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of US Patent No. 6,429,630. Since the cited US patent and the instant application are 100% commonly owned, a Terminal Disclaimer has been enclosed herewith. This Terminal Disclaimer is believed to overcome this rejection.

Examiner also rejected claims 1-18 under 35USC102(b) as being clearly anticipated by Manning US Patent 5,818,780. In the Office Action, Examiner noted that: Manning discloses a first regulator (36), an array of second regulator circuitry (26 and 30) that they are configured to couple a plurality of portions of a microprocessor and these arrays of second regulators are coupled together in parallel.

Applicants respectfully request Examiner's reconsideration and withdrawal of the rejection for the reasons set forth herein. Before addressing the specific features of applicants' invention that provide patentable distinctions over the cited patent, some basic technical distinctions are addressed. It is noted at the outset that the Manning patent is directed to power regulation and distribution in memory devices. At column 1 lines 12-13, Manning states that: This invention relates in general to memory devices, and in particular to memory devices with voltage regulators. See also column 2 lines 46-50 where Manning states: Although the present invention will be described with respect to DRAM, those having skill in the field of this invention will understand that the present invention Is applicable to <u>any memory device</u> which internally regulates a supply voltage. (emphasis added) For this reason, the problem addressed and solved by Manning's patent relates to two aspects of memories (and <u>not</u> microprocessors). First, there is the problem of two different states: 1. a stand-by state requiring low power and 2. an active state requiring high power. Second, there is the problem of long

distribution busses requiring multiple regulation circuits positioned at multiple locations along the distribution busses.

Regarding the problem of two different states, Manning provides low-power regulator circuit 36, presumably optimized to provide low power during a stand-by state. Regarding the problem of long distribution busses, Manning provides a plurality of regulator circuits 26 and 30, connected at various points on the distribution busses 24 and 28, to provide this distributed power to memory cell array 20 and plurality of control circuits 22. All of regulator circuits 26 and 30 are of similar construction as illustrated in FIG. 4 of Manning. Regulator circuit 36 differs only in that it is optimized to decrease power consumption (column 6, lines 17-26). However, since no mention in Manning is made to the contrary, it is presumed that all the regulators provide current to the memory at the same speed. Neither regulator circuits 26 and 30 or regulator 36 are concerned with the speed with which currents are provided because a response to transient events, a common requirement of power supplies for microprocessors, is a problem not addressed in the memory power supply design of Manning.

In contradistinction, applicants addressed and solved problems of power requirements related to microprocessors and related microelectronic devices. In particular, applicants observed that as microprocessor gate counts and clock speeds increase, improved methods and apparatus for supplying high current at high speed and low voltage are desired. In this regard, applicants disclose a variety of regulators, in a tiered power regulation system, to respond to load power demands at different rates. This invention is succinctly claimed, as for example in claim1, as follows:

A tiered power regulation system comprising:

a first power regulator; and

an array comprising a plurality of second power regulators, <u>said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,</u>

wherein said array comprising a plurality of second power regulators is configured to couple to a plurality of portions of a microprocessor. (emphasis added)

Thus, while Manning discusses memory devices, applicants addressed the unique requirements of microprocessors. Applicants' invention provides for a first power regulator (of one type) and a plurality of second power regulators (of another type) configured to respond to a load power demand rate greater than the first power regulator. This is patentably distinct from the two different power levels provided by the power regulators of Manning. Manning has no need to respond to transient current requirements of the type encountered in high speed microprocessors. Manning also has no need for a high speed power regulator to respond to high speed transients while a low speed power regulator cannot respond as fast. Since the memory devices of Manning had no need for the type of current response required by microprocessors, his power regulators did not provide the desired features. Accordingly, applicants' invention is patentably distinct from the teachings of the Manning patent.

Dependent claims 2-8 are believed to be allowable because they depend from an allowable claim and also in that they recite additional features of the invention. For example, there is no teaching in Manning re: bump technology (Claim 2), a compound semiconductor substrate (Claim 3), or a switching regulator (Claim 4). Claim 5 should be allowed as depending from an allowable claim.

Regarding claim 6, note that the low power regulator 36 of Manning provides stand-by power only to the memory array (DRAM). This standby power is required so that the dynamic memory cells do not lose the stored information. However, the control circuits 22 and regulator circuits 26 and 30 require no stand-by power. Thus, there is no teaching in Manning of:

The tiered power regulation system of claim 1, wherein said first regulator provides power to said array and to said microprocessor.

As previously noted, there is no microprocessor in Manning, rather the "load" for the power supply is the memory cell array 20, to which the low-power regulator circuit provides stand-by power. However, the low-power regulator (corresponding to the first regulator in claims 1 and 6) supplies no power to the regulator circuits 26 and 30 (the elements corresponding to "array" in claim 6) or to control circuits 22. Thus, in addition to depending from an allowable claim, claim 6 recites features distinct from and patentable over Manning.

Regarding claim 7, Manning has no teaching related to the advantages of using discrete electronic components. Regarding claim 8, there is no teaching in Manning to the overall combination with claim 1.

In claim 9, applicants recite:

A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands. (emphasis added)

As previously noted, there is no teaching in Manning of differently configured power regulators in which the second power regulators respond to a load power demand rate greater than the first power regulators. Dependent claims 10-17 are believed to be allowable for the same reasons and also that they recite additional features of the invention.

Lastly, claim 18 recites:

A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

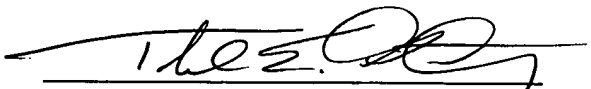
an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,

wherein said array is coupled in parallel to said microelectronic device using bump technology. (emphasis added)

As previously noted, Manning does not teach supplying power to a microelectronic device, but rather a DRAM. Reference to FIGs. 1 and 2 reveals that DRAM 18 and all the regulator circuits are on the same substrate. There is no teaching of having first and second substrates and that the second power regulators formed on a second substrate are configured to respond to a load power demand rate greater than the first regulator responds to power demands.

In view of the foregoing, it is believed that claims 1-18, all the claims currently in this application, are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully requested to telephone the undersigned. An early notification of allowance is earnestly solicited.

Respectfully submitted,
William Pohlman et al



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